Thomas Koetting

Lawrence, KS | 913-375-0261 | tckoetting@gmail.com | LinkedIn | GitHub | Personal Website

Education

Cumulative GPA: 3.7/4.0

University of Kansas — Aug. 2024 - May 2028

Bachelor of Science in Computer Engineering

Relevant Coursework: Digital Logic, FPGA Programming, Embedded Systems, Electric Circuits, Software Design Methodology

Johnson County Community College — Aug. 2022 - May 2024

Technical Skills

Hardware & RTL Design: Verilog, VHDL, RTL Architecture, Microarchitecture, Datapath & Control Logic, FSM Design, Static Timing Analysis (STA) basics

EDA & Simulation Tools: AMD Vivado, Icarus Verilog, GTKWave, ModelSim, PSpice

Languages & Scripting: C/C++, Python, RISC-V Assembly, SQL, Bash

Tools & Methodologies: Git, Cycle-Accurate Simulation, Self-Checking Testbenches, Unit Testing, LaTeX

Projects

RISC-V Microcontroller

Video Link | GitHub

- Designed a synthesizable 32-bit RV32I RISC-V processor core in Verilog, implementing instruction fetch, decode, immediate generation, and branch target calculation
- Engineered the execution datapath with a 32-bit multi-operation ALU and a 32-entry dual-read, synchronous-write register file enforcing zero-register (x0) semantics.
- **Produced and published a 43-minute technical architecture video breakdown**, delivering an exhaustive module-by-module walkthrough of the RTL codebase, datapath schematics, and live waveform verification in GTKWave for hiring teams and open-source contributors.

Circular Ring Buffer & PID Controller

- Programmed an embedded circular buffer data structure in C featuring push/pop operations, head/tail pointer tracking, and explicit overflow handling.
- Built a discrete PID control loop using fixed-point arithmetic to eliminate floating-point hardware overhead on resource-constrained microcontrollers

RISC-V MCU I/O Integration & SystemVerilog Verification — In-Progress

- Integrating memory-mapped I/O peripherals into the RV32I core, optimizing datapath control logic to reduce FPGA utilization, developing a SystemVerilog testbench and documenting the architecture and verification methodology and process in a follow-up video.